PTO/SB/30 (11-04)
Approved for use through 07/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PETITION FEE
Under 37 CFR 1.17(f), (g) & (h)
TRANSMITTAL
(Fees are subject to annual revision)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number	**10/766,848**
Filing Date	**January 30, 2004**
First Named Inventor	**T. KOGA, et al**
Art Unit	
Examiner Name	
Attorney Docket Number	**1309.43463X00**

Enclosed is a petition filed under 37 CFR §1.102(d) that requires a processing fee (37 CFR 1.17(f), (g), or (h)). Payment of $ 130.00 is enclosed.

This form should be included with the above-mentioned petition and faxed or mailed to the Office using the appropriate Mail Stop (e.g., Mail Stop Petition), if applicable. For transmittal of processing fees under 37 CFR 1.17(i), see form PTO/SB/17i.

Payment of Fees (small entity amounts are NOT available for the petition (fees)

☒ The Commissioner is hereby authorized to charge the following fees to Deposit Account No. 50-1417:
☐ petition fee under 37 CFR 1.17(f), (g) or (h) ☒ any deficiency of fees and credit of any overpayments
Enclose a duplicative copy of this form for fee processing.

☐ Check in the amount of $ _____ is enclosed.

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Petition Fees under 37 CFR 1.17(f): Fee $400 Fee Code 1462
For petitions filed under:
§ 1.53(e) - to accord a filing date.
§ 1.57(a) - to according a filing date.
§ 1.182 – for decision on a question not specifically provided for.
§ 1.183 – to suspend the rules.
§ 1.378(e) for reconsideration of decision on petition refusing to accept delayed payment of maintenance fee in an expired patent.
§ 1.741(b) – to accord a filing date to an application under §1.740 for extension of a patent term.

Petition Fees under 37 CFR 1.17(g): Fee $200 Fee code 1463
For petitions filed under:
§1.12 - for access to an assignment record.
§1.14 - for access to an application.
§1.47 - for filing by other than all the inventors or a person not the inventor.
§1.59 - for expungement of information.
§1.103(a) - to suspend action in an application.
§1.136(b) - for review of a request for extension of time when the provisions of section 1.136(a) are not available.
§1.295 - for review of refusal to publish a statutory invention registration.
§1.296 - to withdraw a request for publication of a statutory invention registration filed on or after the date the notice of intent to publish issued.
§1.377 – for review of decision refusing to accept and record payment of a maintenance fee filed prior to expiration of a patent.
§1.550(c) – for patent owner requests for extension of time in ex parte reexamination proceedings.
§1.956 – for patent owner requests for extension of time in inter partes reexamination proceedings.
§ 5.12 – for expedited handling of a foreign filing license.
§ 5.15 – for changing the scope of a license.
§ 5.25 – for retroactive license.

Petition Fees under 37 CFR 1.17(h): Fee $130 Fee Code 1464
For petitions filed under:
§1.19(g) – to request documents in a form other than that provided in this part.
§1.84 – for accepting color drawings or photographs.
§1.91 – for entry of a model or exhibit.
§1.102(d) – to make an application special.
§1.138(c) – to expressly abandon an application to avoid publication.
§1.313 – to withdraw an application from issue.
§1.314 – to defer issuance of a patent.

Name (Print/Type)	**Colin D. Barnitz**	*Registration No. (Attorney/Agent)*	**35,061**
Signature	Colin D. Barnitz	*Date*	May 12, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	**10/766,848**	Confirmation No. 4138
Applicant	:	KOGA, T. et al.	
Filed	:	January 30, 2004	
Title	:	FITTING SUBSTRATE FOR CONNECTION AND FITTING SUBSTRATE FOR CONNECTION FOR USE IN DISK ARRAY CONTROL APPARATUS	
TC/AU	:	2827	
Examiner	:	TBD	
Docket No.	:	1309.43463X00	
Customer No.:		24956	

PETITION TO MAKE SPECIAL
UNDER 37 CFR §1.102(d) (MPEP §708.02(VIII))

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

05/13/2005 SZEWDIE1 00000064 10766848
01 FC:1464 130.00 OP

Sir:

The Applicants petition the Commissioner to make the above-identified application special in accordance with 37 CFR §1.102(d). In support of this Petition, pursuant to MPEP § 708.02(VIII), Applicants state the following.

(A) REQUIRED FEE

This Petition is accompanied by the fee set forth in 37 CFR § 1.117(h). A Credit Card Payment Form in the amount of $130 accompanies this Petition in satisfaction of the fee. The Commissioner is hereby authorized to charge any

additional payment due, or to credit any overpayment, to Deposit Account No. 50-1417.

(B) ALL CLAIMS ARE DIRECTED TO A SINGLE INVENTION

Claims 1-10 are pending in the application. All the pending claims of the application are directed to a single invention. If the Office determines that all claims in the application are not directed to a single invention, Applicant will make election without traverse as a prerequisite to the grant of special status.

The claimed invention, as set forth in independent claims 1, 9 and 10, is generally directed to a fitting substrate that is suitable for connection in a disk array control apparatus, or the like. Under independent claim 1, the invention is a fitting substrate for connection to which first and second kinds of signal processing substrates mutually transmitting and receiving signals are fitted, comprising: a substrate main body; first signal connection point groups formed on said substrate main body and connected to said first kind of signal processing substrate; second signal connection point groups formed on said substrate main body and connected to said second kind of signal processing substrate; and wiring pattern groups for electrically connecting mutually corresponding signal connection points of said first and second signal connection point groups to one another; wherein said first and second signal connection point groups are respectively formed so that mutually corresponding signal connection points can be arranged substantially horizontally on

the same plane, and said wiring pattern group is formed substantially linearly to match with the arrangement of each of said signal connection points.

Additionally, under independent claim 9, the invention is a fitting substrate for connection for use in a disk array control apparatus to which memory substrates, bus switch substrates for controlling connection with said memory substrates and adaptor substrates for gaining access to said memory substrates through said bus switch substrates are fitted, comprising: a substrate main body; bus switch signal connection point groups formed on said substrate main body and connected to said bus switch substrates; adaptor signal connection point groups formed on said substrate main body and connected to said adaptor substrates; and wiring pattern groups for electrically connecting mutually corresponding signal connection points of said bus switch signal connection point group and said adaptor signal connection point group; said bus switch signal connection point group and said adaptor signal connection point group being formed in such a fashion that said mutually corresponding signal connection points are arranged substantially horizontally on the same plane; said wiring pattern group being formed substantially linearly to match with the arrangement of each of said signal connection points.

Furthermore, under independent claim 10, the invention is a disk array control apparatus comprising: a fitting substrate for connection; memory substrates fitted to one of the surfaces of said fitting substrate for connection; bus switch substrates fitted to said one surface, for controlling connection with said memory substrates; and adaptor substrates fitted to said one surface, for gaining access to said memory

substrates through said bus switch substrate; said fitting substrate for connection including: bus switch signal connection point groups connected to said bus switch substrates; adaptor signal connection point groups connected to said adaptor substrates; and wiring pattern groups for electrically connecting mutually corresponding signal connection points of said bus switch signal connection point group and said adaptor signal connection point group; said bus switch signal connection point group and said adaptor signal connection point group being formed in such a fashion that said mutually corresponding signal connection points are arranged substantially horizontally on the same plane; said wiring pattern group being formed substantially linearly to match with the arrangement of each of said signal connection points.

(C) PRE-EXAMINATION SEARCH

A careful and thorough pre-examination search has been conducted, directed to the invention as claimed. The pre-examination search was conducted in the following US Manual of Classification areas:

Class	Subclass
174	52.4, 261
361	684, 729, 752, 760, 764, 772, 773
361	777, 782, 783, 785, 788, 796, 803, 807, 820
370	380, 386
439	61, 65

Furthermore, a keyword search was conducted on the USPTO's EAST database, including the US patent database, the US published patent applications database, and the European and Japanese abstract databases.

(D) DOCUMENTS DEVELOPED BY THE PRE-EXAMINATION SEARCH AND OTHER ART OF RECORD IN THE APPLICATION

The documents located by the pre-examination search are listed below. These documents were made of record in the present application by the Information Disclosure Statement filed April 21, 2005.

Document No.	Inventor
US 4866508	Eichelberger et al.
US 4868634	Ishida et al.
US 4942453	Ishida et al.
US 4994902	Okahashi et al.
US 5388099	Poole
US 5420756	Katsumata et al.
US 6392142	Uzuka et al.
US 20020074670	Suga
US 20040090758	Horikawa

Additionally, the following document was made of record in the present application by the Information Disclosure Statement filed January 30, 2004.

Document No.	Inventor
JP 11-312854	Uzuka et al.

Because all of the above-listed documents are already of record in the present application, in accordance with MPEP § 708.02(VIII)(D), additional copies of these documents have not been submitted with this Petition.

(E) DETAILED DISCUSSION OF THE REFERENCES

Those of the above-listed documents deemed to be most closely-related to the present matter encompassed by the claims are discussed below in section 2, pointing out, with the particularity required by 37 CFR 1.111 (b) and (c), how the claimed present matter is patentable over the teachings of these documents.

1. Discussion of the Invention

Under the invention, a fitting substrate for a disk array apparatus includes first and second kinds of signal processing substrates (e.g., bus switch substrates and adaptor substrates) with signal connection point groups formed in-line so that a connecting wiring pattern group is formed substantially linearly. The linear arrangement of the wiring pattern group improves signal quality and allows higher mounting density. (See, e.g., FIGS. 9A and 9B, and specification at pages 37-39.)

Accordingly, it is submitted that the present invention is patentable over the cited references, since the independent claims of the present application provide for a fitting substrate with first signal connection point groups connected to a first substrate and second signal connection point groups connected to a second substrate so that mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points, as set forth in independent claims 1, 9 and 10.

As will be discussed in more detail below, the prior art does not teach or suggest the above-described features which are useful for improving performance and increasing density of substrates in a disk array system.

2. Discussion of the References Deemed to be Most-Closely Related

The patent to Eichelberger et al., US 4866508, shows a high-density interconnect method in which integrated circuit chips are positioned to take full advantage of a wiring layer that includes a plurality of periodically interrupted conductor patterns. FIG. 2 shows main channel wiring 30, which comprises conductors disposed on 1 mil centers oriented horizontally. These conductors are interrupted between each pair of chips mounted on a substrate. (See, e.g., Abstract, column 3, line 62, through column 5, line 37, and column 7, lines 25-41.) However, Eichelberger et al. do not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

The first patent to Ishida et al., US 4868634, discloses an inclined arrangement of IC chips allows the wiring patterns between common connecting terminals to be arranged in a substantially linear shape. The IC-packaged device

comprises a lower plate which has wiring patterns at least on an upper surface; an upper plate which has upper surface wiring patterns and at least an opening hole and are superimposed on the lower plate when used; and a plurality of IC chips which has a lot of connecting terminal groups mounted on the upper plate. In this structure, some of the connecting terminal groups of the plurality of IC chips are wire-bonded to the wiring patterns on the upper plate, while the other of the connecting terminal groups of the plurality of IC chips pass through the opening hole in the upper plate and are wire-bonded directly to the wiring patterns on the lower plate. (See, e.g., Abstract and column 2, line 54 through column 3, line 60, and column 5, lines 5-32.) However, unlike the present invention, Ishida et al. does not disclose a fitting substrate for connection to first and second kinds of signal processing substrates. Thus, Ishida et al. do not teach not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

The second patent to Ishida et al., US 4942453, discloses memory IC chips in a package that are connected together by a linear wiring pattern. The memory IC chips have a plurality of common connecting terminals on a main circuit board. The plurality of IC chips are packaged on an auxiliary board to make an IC chip unit, and

a plurality of IC chip units are aligned on the main circuit board. The connections between unit-connecting terminals provided on the respective IC chip units and the main circuit board are made by means of wiring patterns on the main circuit board. (See, e.g., Abstract, column 5, lines 47-57, column 7, lines 20-25, and FIG. 5A.) However, unlike the present invention, Ishida et al. does not disclose a fitting substrate for connection having first and second kinds of signal processing substrates. Thus, Ishida et al. do not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

The patent to Okahashi et al., US 4994902, discloses an electronic system having a first and a second semiconductor device acting as a microprocessor and a coprocessor, respectively, disposed linearly on a mounting board. The external pins common to both the first and the second semiconductor devices are connected by wiring means installed linearly on the mounting board. The linear connection may reduce skews in clock signals exchanged between the microprocessor and its coprocessor or between a plurality of coprocessors, and can reduce crosstalk. (See, e.g., Abstract, column 2, lines 15-33, column 10, line 37, through column 11, line 56, and FIGS. 9 and 10.) However, unlike the present invention, Okahashi et al. does

not disclose a fitting substrate for connection having first and second kinds of signal processing substrates. Thus, Okahashi et al. do not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

The patent to Poole, US 5388099, discloses line cards that are connected to the backplane wiring arrangement in a hub. Each line card has receive ports and transmit ports arranged in a regular linear pattern on an edge of each of the line cards. The receiving ports and transmitting ports are arranged in a regular linear pattern on each edge of each of the line cards, and connectors in the slots for the transmitting and receiving ports on an edge of each of the line cards are physically arranged in a regular matrix pattern. The backplane wiring paths are configured diagonally, and the transmit-left ports are all at one end of the linear pattern, and the transmit right ports are all at the other end of the linear pattern. (See, e.g., Abstract, column 2, lines 13-41, and column 9, lines 10-34.) However, unlike the present invention, Poole does not disclose a fitting substrate for connection having first and second kinds of signal processing substrates. Thus, Poole does not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively,

wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

The patent to Katsumata et al., US 5420756, discloses an interconnection of semiconductor memory elements which are connected in a straight wiring pattern on a circuit board. Each semiconductor memory element has outer leads on its one side surface. The outer leads having the same function are arranged in a straight line on the front or rear surface of the print substrate. The outer leads arranged in the straight line are connected with each other via a straight wiring pattern. (See, e.g., Abstract, column 1, line 43, through column 2, line 15, and column 4, lines 22-62.) However, unlike the present invention, Katsumata et al. does not disclose a fitting substrate for connection having first and second kinds of signal processing substrates. Accordingly, Katsumata et al. do not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

The published patent application to Suga, US 20020074670, discloses a semiconductor device in which a plurality of semiconductor substrates, each carrying

semiconductor elements, are bonded together, wherein an insulating layer is deposited on each semiconductor substrate, there being formed a connection wiring passing through the insulating layer for connection to a wiring layer on the semiconductor elements, and wherein an electrically conductive layer of an electrically conductive material, having an opening formed by patterning in register with the connection wiring, is formed on a junction surface of at least one of the semiconductor substrates. The semiconductor substrates are bonded together to interconnect the connection wirings formed on each semiconductor substrate. The semiconductor substrates are connected together with short and straight wirings to take measures against noise. (See, e.g., Abstract and paragraph 11.) However, unlike the present invention, Suga does not disclose a fitting substrate for connection having first and second kinds of signal processing substrates. Thus, Suga does not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

The published patent application to Horikawa, US 20040090758, discloses a semiconductor device in which a semiconductor element and chip capacitor are connected with each other by linear conductor paths, so that the occurrence of

switching noise can be effectively reduced and electric power can by supplied to the semiconductor element in a stable fashion. (See, e.g., Abstract and paragraphs 8-11.) However, unlike the present invention, Horikawa does not disclose a fitting substrate for connection having first and second kinds of signal processing substrates. Thus, Horikawa does not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points

3. Remaining References

The remaining references of record in the application are deemed to not be most-closely related to the present invention, and/or were provided as background information, and also do not show or suggest the present invention. However, a discussion of the remaining references has been provided to avoid dismissal of the Petition in case the Examiner disagrees with Applicants' determination that these references are not most-closely related to the subject matter of the claims.

The US Patent to Uzuka et al., US 6392142 (US equivalent of JP 11-312854), shows a printed wiring board mounting structure. As also discussed in the specification of the present application, beginning at page 2, Uzuka teaches a

plurality of front-surface-side printed wiring boards and a plurality of rear-surface-side printed wiring boards. The mountings of the rear-surface-side printed wiring boards are orthogonal to those of the front-surface-side wiring boards. Thus, Uzuka et al. do not teach a fitting substrate having first and second substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points.

CONCLUSION

From the above discussion, it is apparent that none of the art of record shows or suggests the present invention, including a fitting substrate having first and second signal processing substrates, as set forth in claims 1, 9 and 10, including first and second signal connection point groups connected, respectively, wherein mutually corresponding signal connection points are arranged substantially horizontally on the same plane, and a wiring pattern group is formed substantially linearly to match with the arrangement of each of the signal connection points. Accordingly, claims 1, 9 and 10 are patentable over the cited references.

The Applicants submit that the foregoing discussion demonstrates the patentability of the independent claims over the closest-known prior art, taken either singly, or in combination. The remaining claims depend from the independent

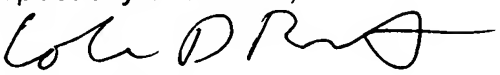
claims, claim additional features of the invention, and are patentable at least because they depend from allowable base claims. Accordingly, the requirements of 37 CFR §1.102(d) having been satisfied, the Applicants request that this Petition to Make Special be granted and that the application be examined according to prescribed procedures set forth in MPEP §708.02 (VIII).

The Applicants prepared this Petition in order to satisfy the requirements of 37 C.F.R. §1.102(d) and MPEP §708.02 (VIII). The pre-examination search required by these sections was "directed to the invention as claimed in the application for which special status is requested." MPEP §708.02 (VIII). The search performed in support of this Petition is believed to be in full compliance with the requirements of MPEP §708.02 (VIII); however, Applicants make no representation that the search covered every conceivable search area that might contain relevant prior art. It is always possible that prior art of greater relevance to the claims may exist. The Applicants urge the Examiner to conduct his or her own complete search of the prior art, and to thoroughly examine this application in view of the prior art cited above and any other prior art that may be located by the Examiner's independent search.

Further, while the Applicants have identified and discussed certain portions of each cited reference in order to satisfy the requirement for a "detailed discussion of the references, which discussion points out, with the particularly required by 37 C.F.R. §1.111(b) and (c), how the claimed subject matter is patentable over the references" (MPEP §708.02(VIII)), the Examiner should not limit review of these

documents to the identified portions, but rather is urged to review and consider the entirety of each reference.

Respectfully submitted,



Colin D. Barnitz
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Attorney for Applicants

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Date: May 12, 2005

1309.43463X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Tsutomu KOGA, et al

Serial No.: 10/766,848

Filed: January 30, 2004

For: FITTING SUBSTRATE FOR CONNECTION AND FITTING SUBSTRATE FOR CONNECTION FOR USE IN DISK ARRAY CONTROL APPARATUS

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97 & 1.98

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 21, 2005

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

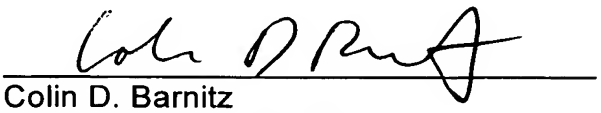
This information disclosure statement is being submitted before the mailing date of a first office action on the merits.

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (1309.43463X00) please credit any excess fees to such deposit account.

Respectfully submitted,



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FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
1309.43463X00	10/766,848
APPLICANT: T. KOGA, et al	
FILING DATE: January 30, 2004	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		4866508	9/89	Eichelberger et al			
		4868634	9/89	Ishida et al			
		4942453	7/90	Ishida et al			
		4994902	2/91	Okahashi et al			
		5388099	2/95	Poole			
		5420756	5/95	Katsumata et al			
		6392142	5/02	Uzuka et al			
	2002	0007467	6/02	Suga			
	2004	0090758	5/04	Horikawa			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT YES	ABSTRACT NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Form PTO-1449 [6-4])

1309.43463X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Tsutomu KOGA, et al

Serial No.: Not Yet Assigned

Filed: On Even Date

For: FITTING SUBSTRATE FOR CONNECTION AND FITTING SUBSTRATE FOR CONNECTION FOR USE IN DISK ARRAY CONTROL APPARATUS

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Mail Stop DD
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 30, 2004

Sir:

In the matter of the above-identified application, applicants are submitting herewith a copy of the document listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

To the extent the document listed on the attached form equivalent to Form PTO-1449 is not in the English language, the requirement of 37 CFR 1.98(a)(3) for a concise explanation of the relevance is satisfied by the discussion of this document in the specification, for example, on page 2.

It is respectfully requested that this information disclosure statement be

considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (Case: 1309.43463X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS LLP

John D Rant

Reg No. 35061

FOR: Melvin Kraus
Registration No. 22,466

MK/nac
(703) 312-6600

Attachments

PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	
Filing Date	January 30, 2004
First Named Inventor	KOGA, TSUTOMU
Art Unit	
Examiner Name	
Attorney Docket Number	1309.43463X00

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]–Number[4]–Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP-11-312854	11-09-1999			

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.